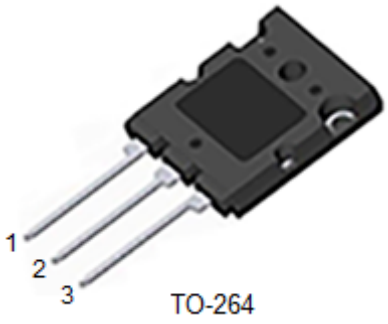
1. Features

- Advanced Planar Process
- $R_{DS(ON)}$=380mΩ(typ.)@V_{GS}=10V
- Low Gate Charge Minimize Switching Loss
- Rugged Poly silicon Gate Structure

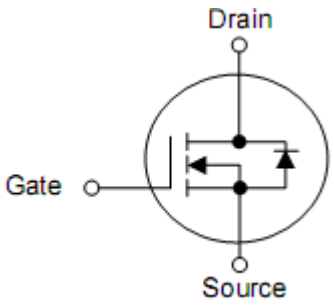
2. Applications

- BLDC Motor Driver
- Electric Welder
- High Efficiency SMPS

3. Symbol



TO-264



Pin	Function
1	Gate
2	Drain
3	Source

4. Ordering Information

Part Number	Package	Brand
KNK75100A	TO-264	KIA

5. Absolute maximum ratings

T_C=25°C unless otherwise noted

Parameter		Symbol	Rating	Units
Drain-source voltage [1]		V_{DSS}	1000	V
Gate-to-Source Voltage		V_{GSS}	±30	V
Continuous drain current	T_C=25°C	I_D	24	A
	T_C=100°C	I_D	15	A
Pulsed Drain Current at V_{GS}=10V [2),4)]		I_{DM}	96	A
Single pulse avalanche energy（L=0.5mH）		E_{AS}	2500	mJ
Peak Diode Recovery dv/dt [3)]		dv/dt	5.0	V/ns
Power dissipation		P_D	650	W
Derate above 25°C			5.44	W/°C
Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10 seconds, Package Body for 10 seconds		T_L T_{PAK}	300 260	°C
Operating junction and storage temperature range		T_J ,T_{STG}	-55 to150	ºC

Caution: Stresses greater than those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device.

6. Thermal characteristics

Parameter	Symbol	Rating	Unit
Thermal resistance junction-case	$R_{\theta JC}$	0.192	ºC/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	55	ºC/W

7. Electrical characteristics

(T_J=25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain-source breakdown voltage	BV_{DSS}	V_{GS}=0V,I_D=250uA	1000	-	-	V
Drain-source leakage current	I_{DSS}	V_{DS}=1000V, V_{GS}=0V	-	-	5	uA
		V_{DS}=800V, T_C=125°C	-	-	125	
Gate-source forward leakage	I_{GSS}	V_{GS}=±30V, V_{DS}=0V	-	-	±100	nA
Drain-source on-resistance 3)	$R_{DS(on)}$	V_{GS}=10V,I_D=12A	-	380	450	mΩ
Gate threshold voltage	$V_{GS(TH)}$	V_{DS}=V_{GS},I_D=250uA	2.5	-	4.5	V
Forward Transconductance	g_{FS}	V_{DS}=25V, I_D=12A	-	18	-	S
Input capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V f=1MHz	-	7300	-	pF
Reverse transfer capacitance	C_{rss}		-	52	-	pF
Output capacitance	C_{oss}		-	552	-	pF
Total gate charge	Q_g	V_{DD}=500V, I_D=12A V_{GS}=0~10V	-	180	-	nC
Gate-source charge	Q_{gs}		-	50	-	nC
Gate-drain charge	Q_{gd}		-	60	-	nC
Turn-on delay time	$t_{d(on)}$	V_{DD}=500V,V_{GS}=10V, R_G=10Ω, I_D=12A	-	68	-	ns
Rise time	t_r		-	118	-	ns
Turn-off delay time	$t_{d(off)}$		-	100	-	ns
Fall time	t_f		-	110	-	ns
Continuous Source Current 2)	I_{SD}	Integral PN-diode in MOSFET	-	-	24	A
Pulsed Source Current2)	I_{SM}		-	-	96	A
Diode forward voltage	V_{SD}	I_S=24A,V_{GS}=0V,	-	-	1.5	V
Reverse Recovery Time	t_{rr}	V_{GS}=0V,I_F=24A, dI_F/dt=100A/μs	-	900	-	nS
Reverse Recovery Charge	Q_{rr}		-	2.0	-	uC

Note:
1) T_J=+25°C to +150°C.
2) Silicon limited current only.
3) Package limited current.
4) Repetitive rating; pulse width limited by maximum junction temperature.
5) Pulse width≤380μs; duty cycle≤2%.

8. Typical operating characteristics

Figure 1. Maximum Transient Thermal Impedance

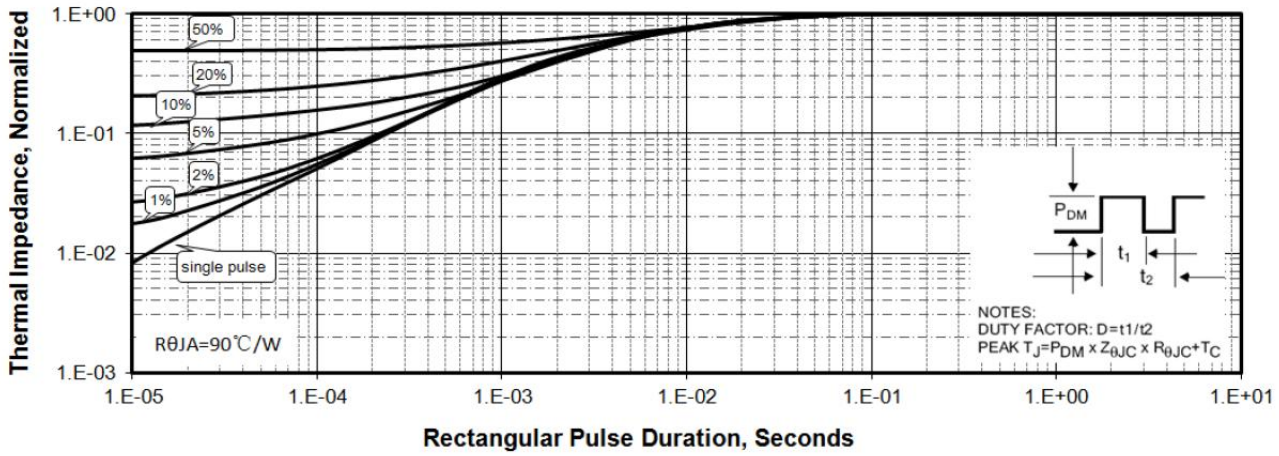


Figure 2 . Max. Power Dissipation vs Case Temperature

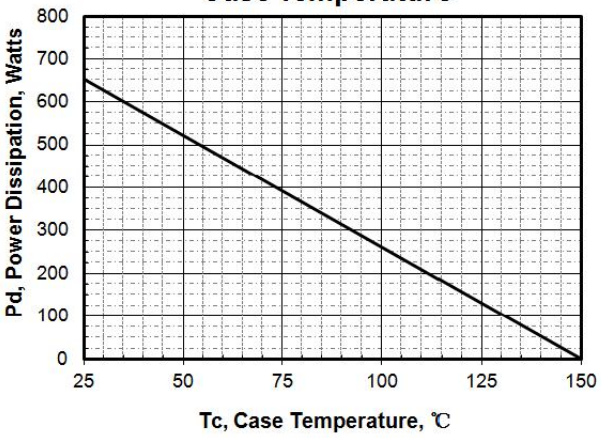


Figure 3 .Maximum Continuous Drain Current vs Tc

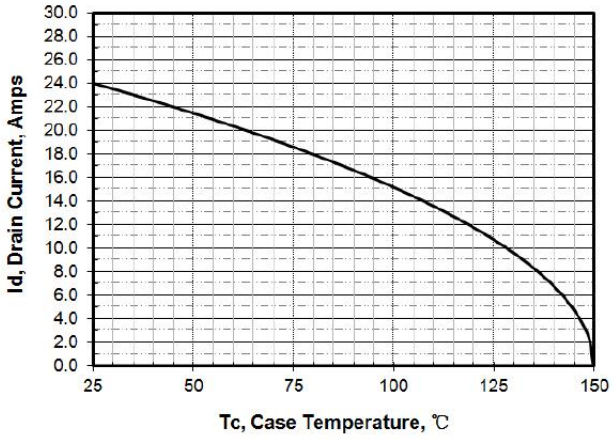


Figure 4. Output Characteristics

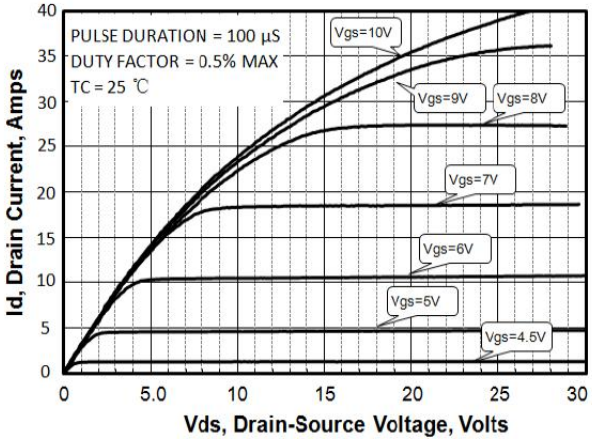


Figure 5. Rdson vs Gate Voltage

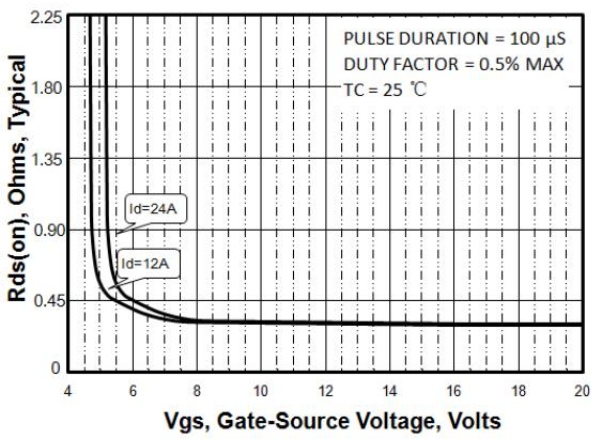


Figure 6. Peak Current Capability

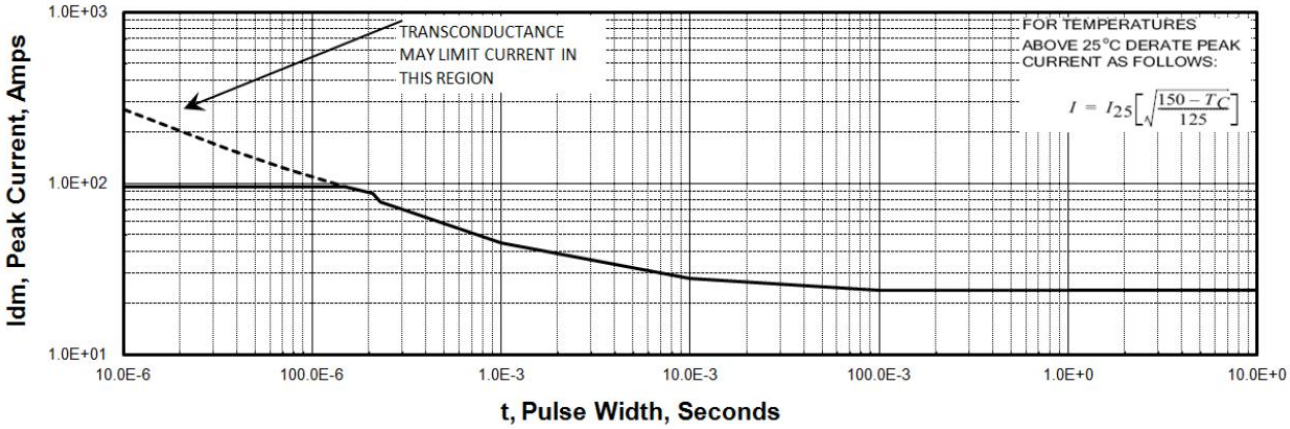


Figure 7. Transfer Characteristics

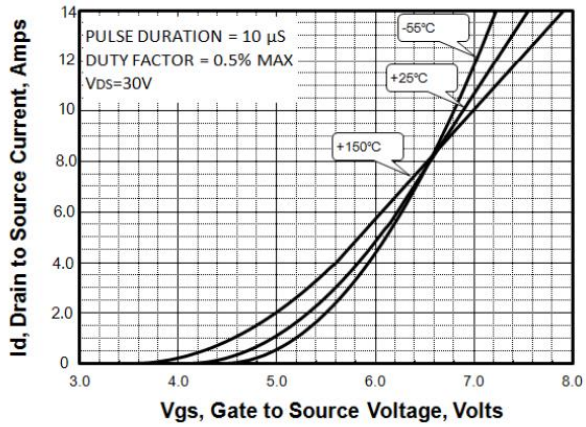


Figure 8. Unclamped Inductive Switching Capability

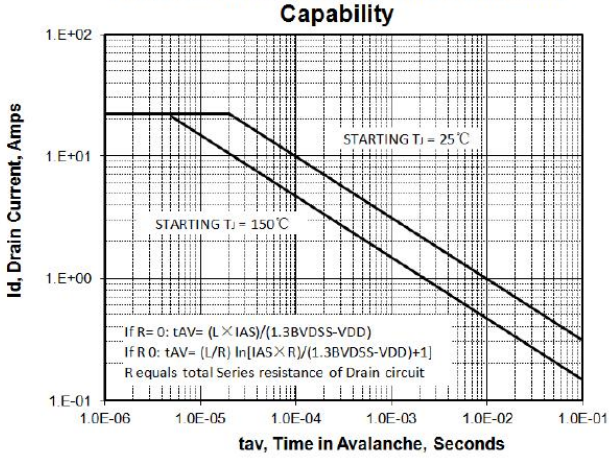


Figure 9. Drain to Source ON Resistance vs Drain Current

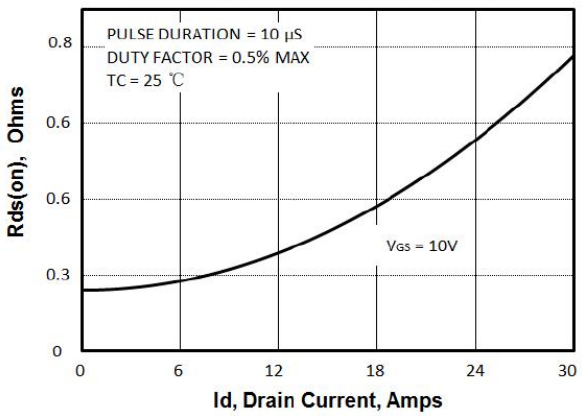


Figure 10. Rdson vs Junction Temperature

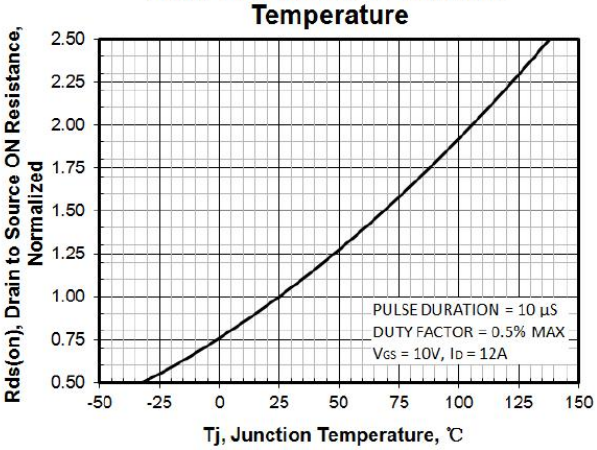


Figure 11.Breakdown Voltage vs Temperature

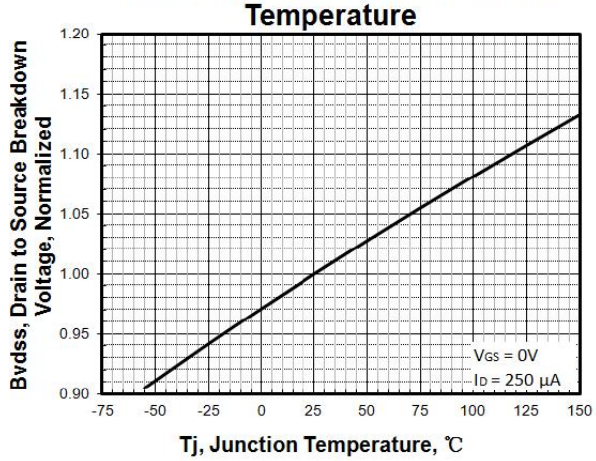


Figure 12.Threshold Voltage vs Temperature

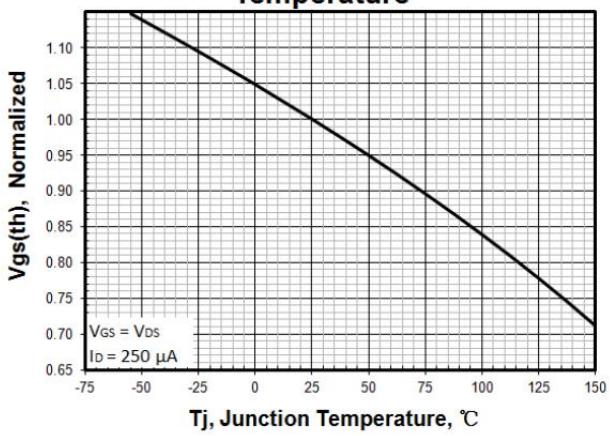


Figure 13 . Maximum Safe Operating Area(TO-220F)

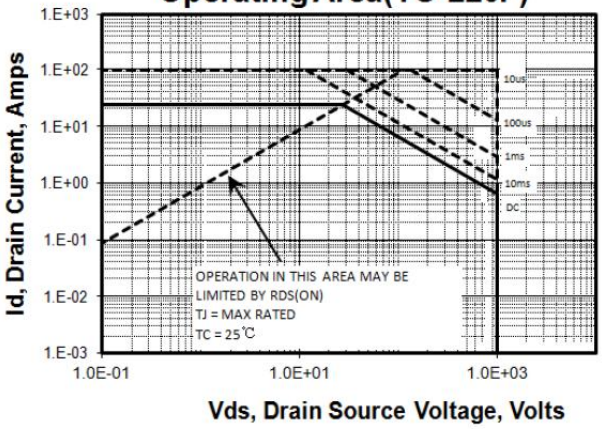


Figure 14. Capacitance vs Vds

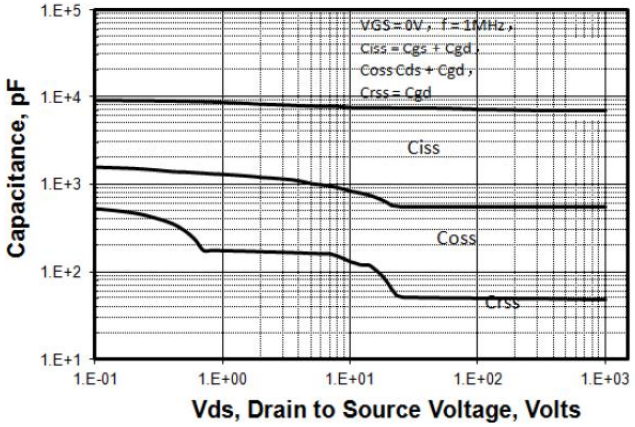


Figure 15 .Typical Gate Charge

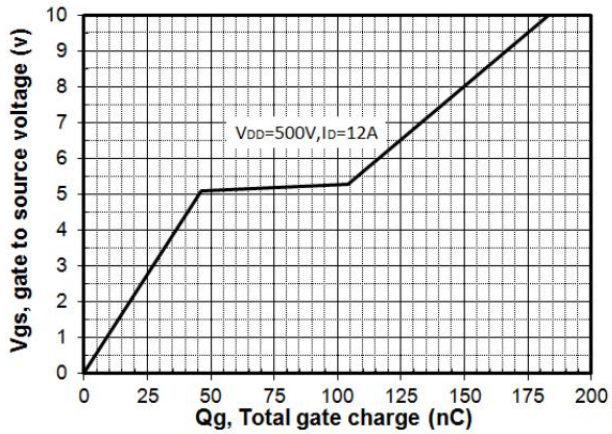
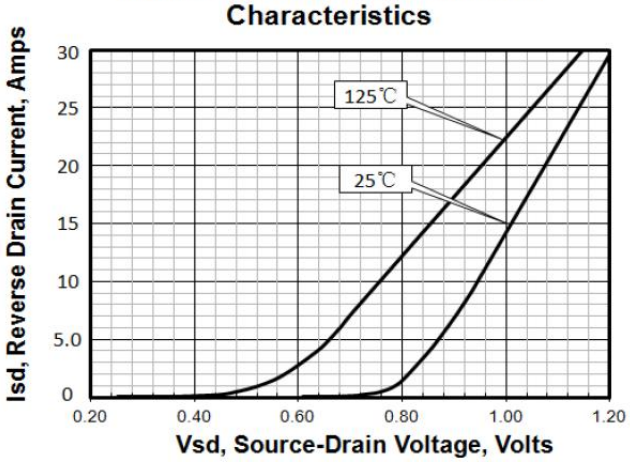


Figure 16.Body Diode Transfer Characteristics



9. Test Circuits and Waveforms

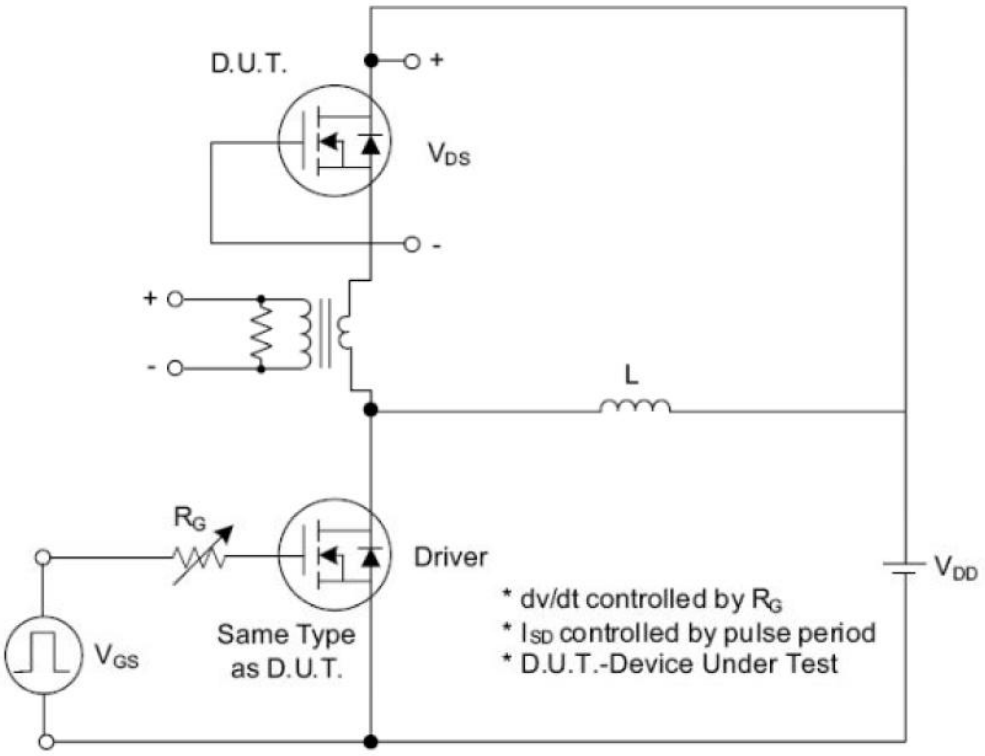


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

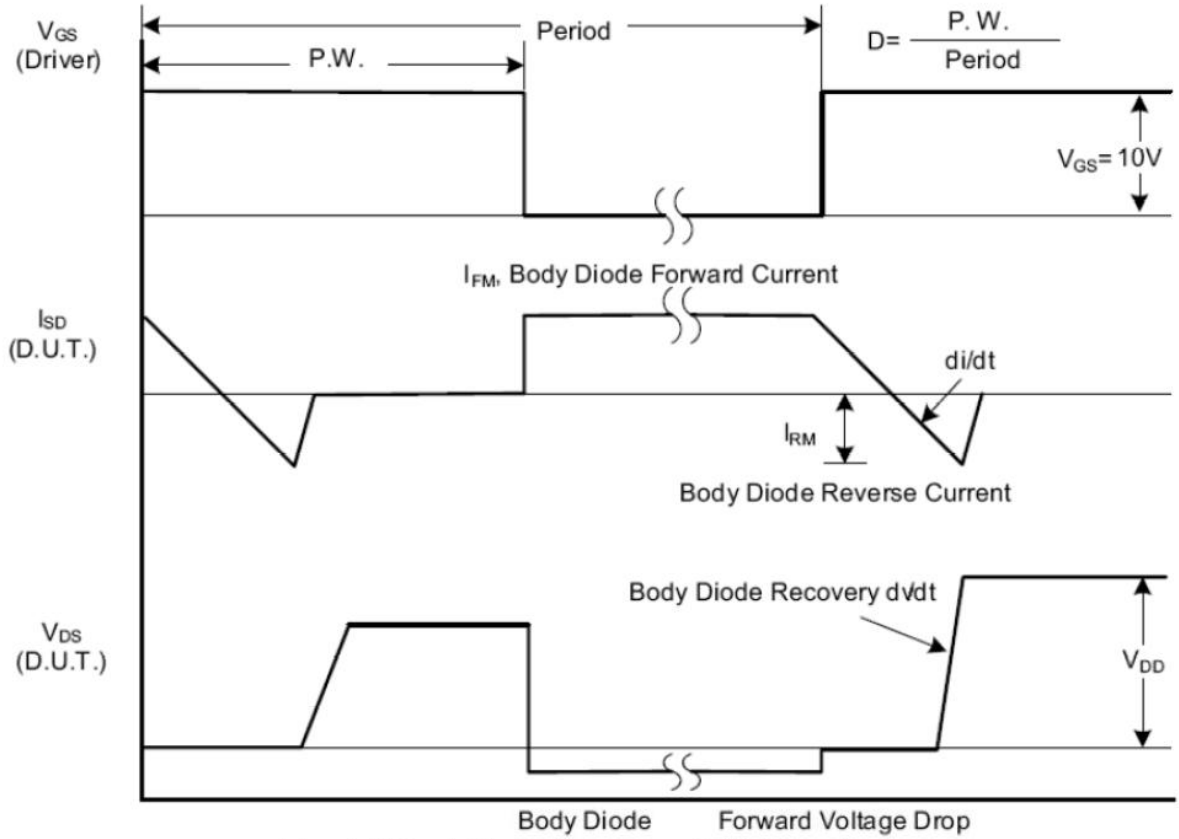


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

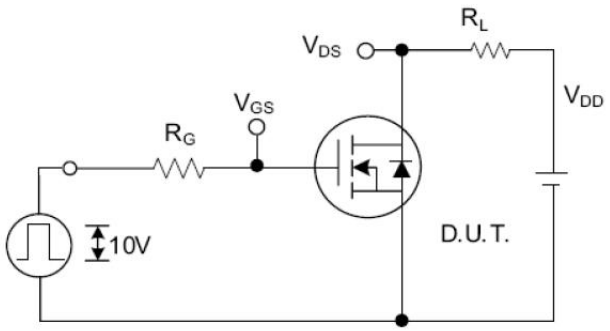


Fig. 2.1 Switching Test Circuit

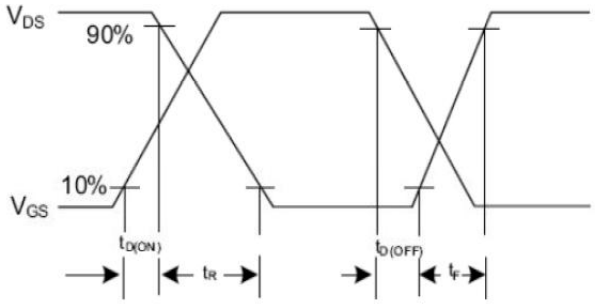


Fig. 2.2 Switching Waveforms

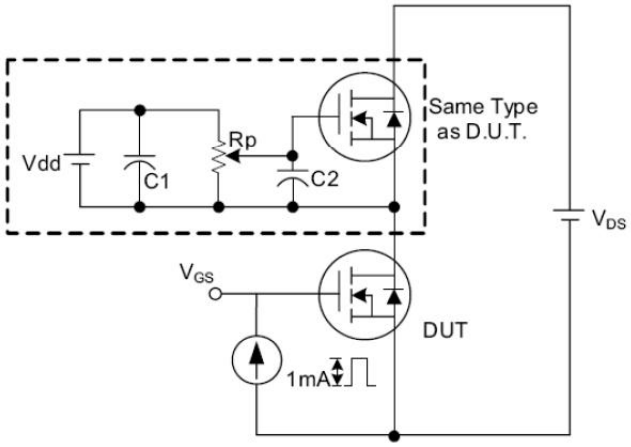


Fig. 3 . 1 Gate Charge Test Circuit

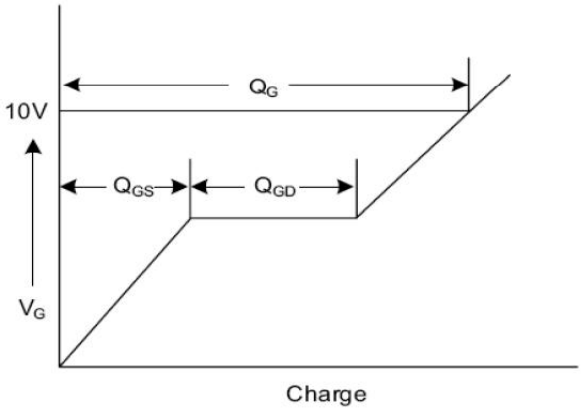


Fig. 3 . 2 Gate Charge Waveform

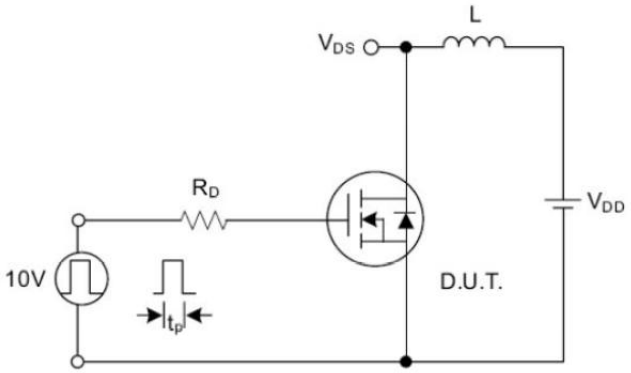


Fig. 4.1 Unclamped Inductive Switching Test Circuit

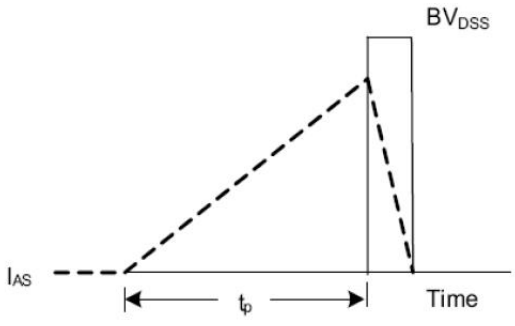


Fig. 4.2 Unclamped Inductive Switching Waveforms